Isaac B Goss

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Experience

Concurrent EDA, LLC | Pittsburgh, PA — May 2018 - Present

- Software and FPGA Engineer
- Implemented 80,000 frame-per-second video capture system
- Developed bare-metal controller firmware for DMA and Ethernet hardware
- Modified Ethernet driver to support 4-port client board
- Maintained embedded Linux systems and applications on smart camera hardware
- Assisted integrating FPGAs onto custom client circuit boards
- Implemented OpenVX image processing functions on FPGA hardware

University of Pittsburgh | Pittsburgh, PA — Aug 2017 - May 2018

- Teaching Assistant: Digital Systems Lab & Advanced Digital Design
- Helped students understand and debug projects
- Graded student projects, papers, and exams

Center for High-Performance and Re-configurable Computing | Pittsburgh, PA — May 2017 - Aug 2017

- Research Intern
- Investigated trade-offs for embedded sensor networks
- Designed Bus-Functional Models for FPGA simulation

Education

University of Pittsburgh | Pittsburgh, PA | GPA: 3.24 / 4.0 — May 2018

- Bachelor of Science in Computer Engineering
- Minor in Mathematics

Relevant Courses

Senior Design, Operating Systems, Cyber-Physical Systems (IoT), Software Engineering, Algorithm Design, Compiler Design, Combinatorics, Computer Architecture, Advanced Digital Design, Graph Theory, Algorithm Implementation, System Software

Languages	**Tools**	**Technologies**
C/C++	git/GitLab	Linux
Python	make	Xilinx FPGAs
Java	TravisCI	Embedded ARM
VHDL	CMake	Ethernet
Bash scripting	LaTeX	Regular Expressions

Projects

ParkPal — Jan 2018 - April 2018

- System to observe and display currently open parallel parking spaces
- Embedded camera installed above street; sends images over WiFi
- Server accepts new images; uses computer vision to find open spaces
- Available spaces are displayed to user in Web interface

Training Montage — Aug 2017 - Dec 2017

- Train control system and simulator application
- Track system and train physics are modeled in simulation
- Centralized and local controller logic emulate a deliverable system
- 5-person agile team, using continuous integration, IEEE documentation

MIPS CPU — Jan 2017 - April 2017

- 5-Stage Harvard pipeline, with full forwarding, and hazard detection
- Constructed from stratch, only using VHDL primitives
- Built with HDL Designer; simulated using ModelSim